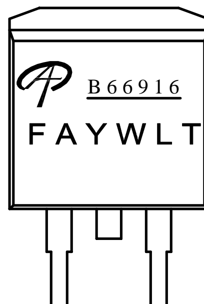
ALPHA & OMEGA SEMICONDUCTOR

Document No.	PD-03092
Version	A
Title	AOB66916L Marking Description

TO263(D2PAK) PACKAGE MARKING DESCRIPTION



Standard product

NOTE:

LOGO	- AOS Logo
B66916	- Part number code
F	- Fab code
A	- Assembly location code
Y	- Year code
W	- Week code
L&T	- Assembly lot code

PART NO.	DESCRIPTION	CODE
AOB66916L	Standard product	B66916

ALPHA & OMEGA SEMICONDUCTOR

Document No.	PO-00005
Version	M

TO263(D2PAK) PACKAGE OUTLINE

A E L1 D Optional L2 3 X b2 2 X b ⌖ 0.25mm Ⓜ B A Ⓜ

B A c2 H SEE VIEW C c A2

E1 ⌖ 0.25mm Ⓜ B A Ⓜ

0°-8° GAUGE PLANE B SEATING PLANE L A1 L3

VIEW C

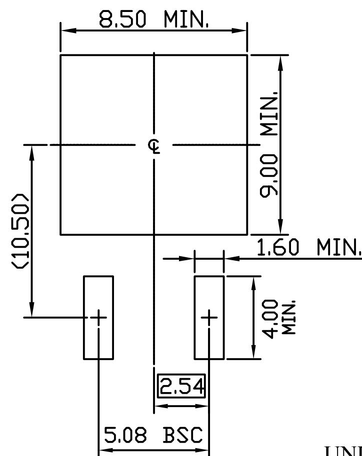
D1 Detail D 2 X e

BOTTOM VIEW

Option 1 Option 2

DETAIL D

RECOMMENDED LAND PATTERN



UNIT: mm

SYMBOLS	DIMENSIONS IN MILLIMETERS			DIMENSIONS IN INCHES		
	MIN	NOM	MAX	MIN	NOM	MAX
A	4.064	4.45	4.826	0.160	0.175	0.190
A1	0.00	---	0.254	0.000	---	0.010
A2	2.20	2.67	2.90	0.087	0.105	0.114
b	0.508	0.81	0.991	0.020	0.032	0.039
b2	1.143	1.27	1.778	0.045	0.050	0.070
c	0.381	0.50	0.737	0.015	0.020	0.029
c2	1.143	1.27	1.651	0.045	0.050	0.065
D	8.382	9.14	9.652	0.330	0.360	0.380
D1	6.858	8.00	8.37	0.270	0.315	0.330
e	2.54 BSC			0.100 BSC.		
E	9.652	10.03	10.668	0.380	0.395	0.420
E1	6.223	8.00	8.37	0.245	0.315	0.330
H	14.605	15.24	15.875	0.575	0.600	0.625
L	1.778	2.54	2.794	0.070	0.100	0.110
L1	1.02	1.27	1.676	0.040	0.050	0.066
L2	1.27	1.52	1.778	0.050	0.060	0.070
L3	0.25 BSC			0.010 BSC.		

NOTE:
1. PACKAGE BODY SIDES EXCLUDE MOLD FLASH AND GATE BURRS.
   MOLD FLASH SHOULD BE LESS THAN 6 MILS.
2. TOLERANCE 0.10 MILLIMETERS UNLESS OTHERWISE SPECIFIED.
3. DIMENSION L IS MEASURED IN GAUGE LINE.
4. CONTROLLING DIMENSION IS MILLIMETER.
   CONVERTED INCH DIMENSIONS ARE NOT NECESSARILY EXACT.
5. REFER TO JEDEC TO-263 AB.

AOS Semiconductor
Product Reliability Report

AOB66916L, rev A

Plastic Encapsulated Device

ALPHA & OMEGA Semiconductor, Inc

www.aosmd.com

Jan, 2019

This AOS product reliability report summarizes the qualification result for AOB66916L. Accelerated environmental tests are performed on a specific sample size, and then followed by electrical test at end point. Review of final electrical test result confirms that AOB66916L passes AOS quality and reliability requirements. The released product will be categorized by the process family and be routine monitored for continuously improving the product quality.

I. Reliability Stress Test Summary and Results

Test Item	Test Condition	Time Point	Total Sample Size	Number of Failures	Reference Standard
HTGB	Temp = 150°C , Vgs=100% of Vgsmax	168 / 500 / 1000 hours	462 pcs	0	JESD22-A108
HTRB	Temp = 150°C , Vds=100% of Vdsmax	168 / 500 / 1000 hours	462 pcs	0	JESD22-A108
Precondition (Note A)	168hr 85°C / 85%RH + 3 cycle reflow@245°C (MSL 1)	-	4620 pcs	0	JESD22-A113
HAST	130°C , 85%RH, 33.3 psia, Vds = 80% of Vdsmax up to 42V	96 hours	693 pcs	0	JESD22-A110
H3TRB	85°C , 85%RH, Vds = 80% of Vdsmax	1000 hours	693 pcs	0	JESD22-A101
Autoclave	121°C , 29.7psia, RH=100%	96 hours	924 pcs	0	JESD22-A102
Temperature Cycle	-65°C to 150°C , air to air,	1000cycles	924 pcs	0	JESD22-A104
HTSL	Temp = 150°C	1000 hours	693 pcs	0	JESD22-A103
IOL	∆ Tj = 100°C	8572 cycles	693 pcs	0	MIL-STD-750 Method 1037

Note: The reliability data presents total of available generic data up to the published date.
Note A: MSL (Moisture Sensitivity Level) 1 based on J-STD-020

II. Reliability Evaluation

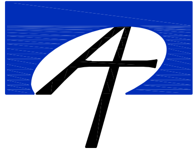
FIT rate (per billion): 3.82
MTTF = 29919 years

The presentation of FIT rate for the individual product reliability is restricted by the actual burn-in sample size. Failure Rate Determination is based on JEDEC Standard JESD 85. FIT means one failure per billion hours.

Failure Rate = $Chi^2 \times 10^9$ **/** **[**2 (N) (H) (Af)**]** **=** 3.82
MTTF = 10^9 / FIT = 29919 years
Chi² = Chi Squared Distribution, determined by the number of failures and confidence interval
N = Total Number of units from burn-in tests
H = Duration of burn-in testing
Af = Acceleration Factor from Test to Use Conditions (Ea = 0.7eV and Tuse = 55°C)
Acceleration Factor [**Af**] = **Exp** [Ea / **k** (1/Tj u – 1/Tj s)]
Acceleration Factor ratio list:

	55 deg C	70 deg C	85 deg C	100 deg C	115 deg C	130 deg C	150 deg C
Af	259	87	32	13	5.64	2.59	1

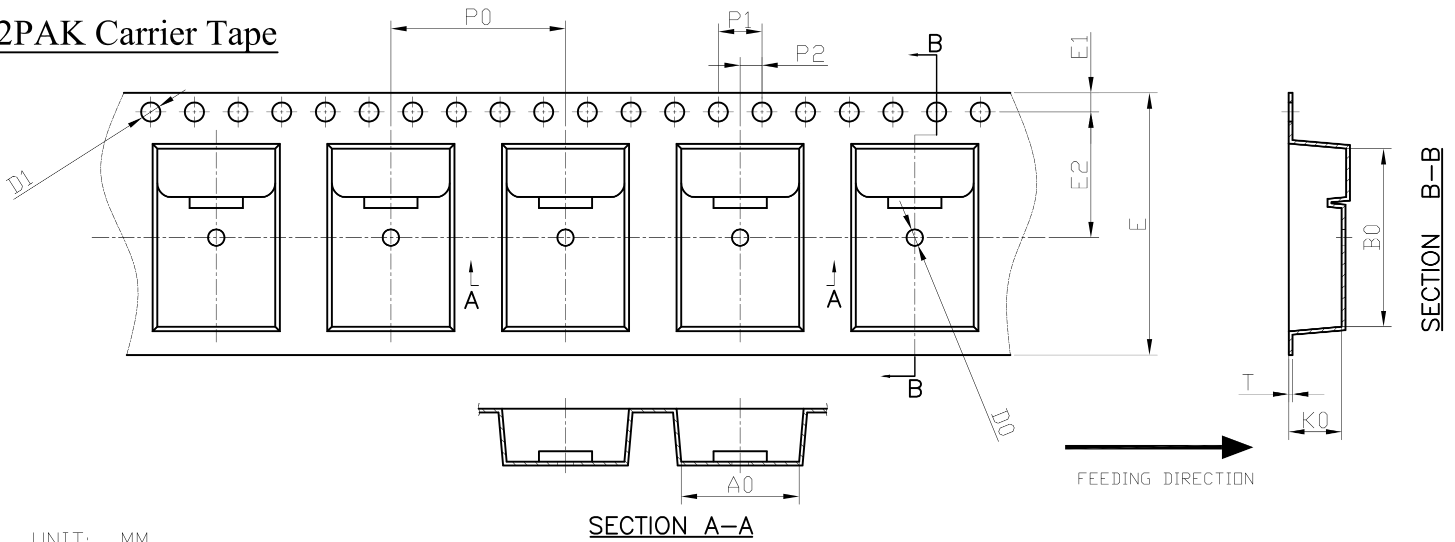
Tj s = Stressed junction temperature in degree (Kelvin), K = C+273.16
Tj u =The use junction temperature in degree (Kelvin), K = C+273.16
k = Boltzmann's constant, 8.617164 X 10^{-5}eV / K



ALPHA & OMEGA SEMICONDUCTOR

D2PAK Tape and Reel Data

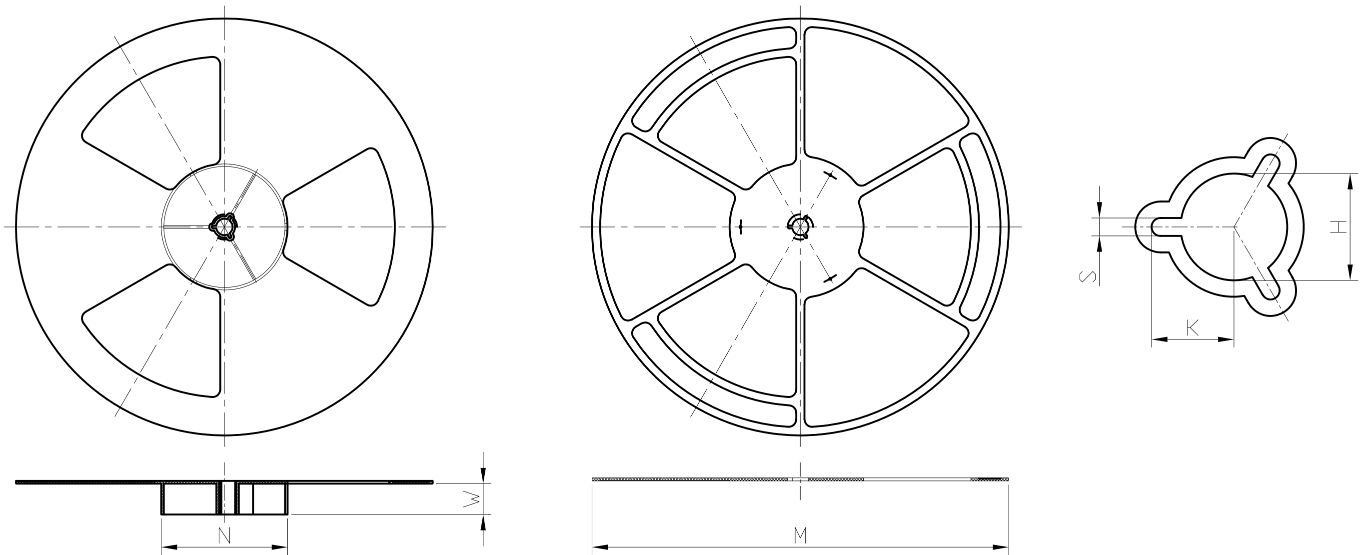
D2PAK Carrier Tape



UNIT: MM

PACKAGE	A0	B0	K0	D0	D1	E	E1	E2	P0	P1	P2	T
D2PAK (24 mm)	10.80 ±0.10	16.30 ±0.10	4.70 ±0.10	1.50 ±0.10	1.50 +0.1 −0	24.00 ±0.30	1.75 ±0.10	11.50 ±0.10	16.00 ±0.10	4.00 ±0.10	2.00 ±0.10	0.35 ±0.10

D2PAK Reel



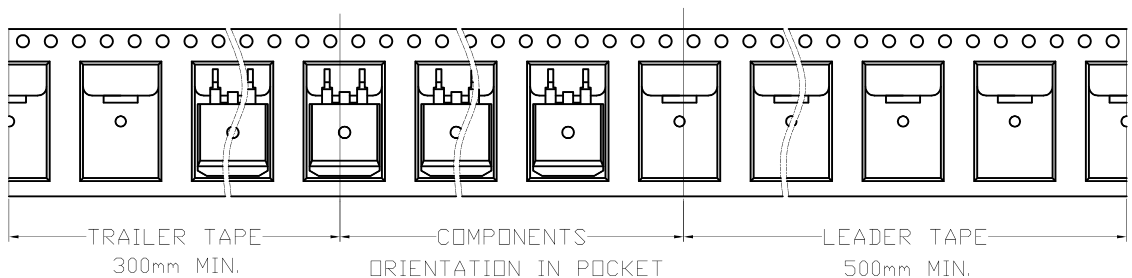
UNIT: MM

TAPE SIZE	REEL SIZE	M	N	W	H	K	S
24 mm	ø330	ø330.00 +0.25 −4.00	ø100.00 ±0.2	24.4 +2.0 −0.0	ø13.00 +0.50 −0.20	10.5 ±0.25	2.2 ±0.25

D2PAK Tape

Leader / Trailer & Orientation

Unit Per Reel: 800pcs



ALPHA & OMEGA SEMICONDUCTOR

AOT66916L/AOB66916L

100V N-Channel AlphaSGT™

General Description

- Trench Power AlphaSGT™ technology
- Best in class on-resistance $R_{DS(ON)}$
- Lowers switching loss by lower Qrr than other MOSFET suppliers
- Optimized voltage spike at SSR application
- RoHS and Halogen-Free Compliant

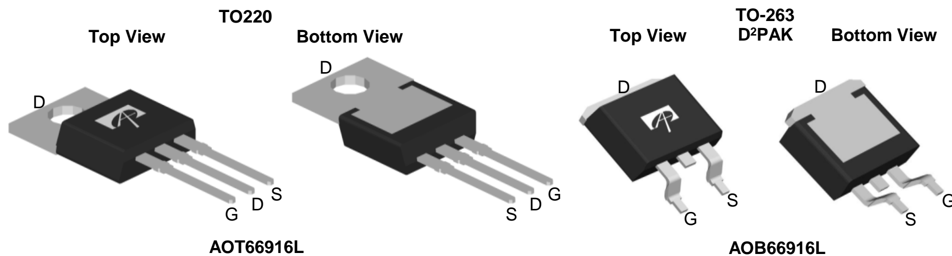
Product Summary

V_{DS}	100V
I_D (at V_{GS}=10V)	120A
$R_{DS(ON)}$ (at V_{GS}=10V)	< 3.6mΩ
$R_{DS(ON)}$ (at V_{GS}=6V)	< 4.8mΩ

100% UIS Tested
100% Rg Tested

Applications

- High frequency switching and synchronous rectification
- BMS
- Motor



Orderable Part Number	Package Type	Form	Minimum Order Quantity
AOT66916L	TO-220	Tube	1000
AOB66916L	TO-263	Tape & Reel	800

Absolute Maximum Ratings T_A=25°C unless otherwise noted

Parameter		Symbol	Maximum	Units
Drain-Source Voltage		V_{DS}	100	V
Gate-Source Voltage		V_{GS}	±20	V
Continuous Drain Current [G]	T_C=25°C	I_D	120	A
	T_C=100°C		120	
Pulsed Drain Current [C]		I_{DM}	450	
Continuous Drain Current	T_A=25°C	I_{DSM}	35.5	A
	T_A=70°C		28.5	
Avalanche Current [C]		I_{AS}	80	A
Avalanche energy	L=0.1mH [C]	E_{AS}	320	mJ
Power Dissipation [B]	T_C=25°C	P_D	277	W
	T_C=100°C		111	
Power Dissipation [A]	T_A=25°C	P_{DSM}	8.3	W
	T_A=70°C		5.3	
Junction and Storage Temperature Range		T_J, T_{STG}	-55 to 150	°C

Thermal Characteristics

Parameter		Symbol	Typ	Max	Units
Maximum Junction-to-Ambient [A]	t ≤ 10s	$R_{\theta JA}$	12	15	°C/W
Maximum Junction-to-Ambient [A D]	Steady-State		50	60	°C/W
Maximum Junction-to-Case	Steady-State	$R_{\theta JC}$	0.35	0.45	°C/W

Electrical Characteristics (T_J=25°C unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
STATIC PARAMETERS						
BV_{DSS}	Drain-Source Breakdown Voltage	I_D=250µA, V_{GS}=0V	100			V
I_{DSS}	Zero Gate Voltage Drain Current	V_{DS}=100V, V_{GS}=0V			1	µA
		T_J=55°C			5	
I_{GSS}	Gate-Body leakage current	V_{DS}=0V, V_{GS}=±20V			±100	nA
$V_{GS(th)}$	Gate Threshold Voltage	V_{DS}=V_{GS}, I_D=250µA	2.5	2.95	3.5	V
$R_{DS(ON)}$	Static Drain-Source On-Resistance	V_{GS}=10V, I_D=20A		3.0	3.6	mΩ
		T_J=125°C		4.9	5.9	
		V_{GS}=6V, I_D=20A		3.6	4.8	mΩ
g_{FS}	Forward Transconductance	V_{DS}=5V, I_D=20A		80		S
V_{SD}	Diode Forward Voltage	I_S=1A, V_{GS}=0V		0.68	1	V
I_S	Maximum Body-Diode Continuous Current [G]				120	A
DYNAMIC PARAMETERS						
C_{iss}	Input Capacitance	V_{GS}=0V, V_{DS}=50V, f=1MHz		6180		pF
C_{oss}	Output Capacitance			1660		pF
C_{rss}	Reverse Transfer Capacitance			29		pF
R_g	Gate resistance	f=1MHz	0.7	1.5	2.3	Ω
SWITCHING PARAMETERS						
$Q_g(10V)$	Total Gate Charge	V_{GS}=10V, V_{DS}=50V, I_D=20A		78		nC
Q_{gs}	Gate Source Charge			22		nC
Q_{gd}	Gate Drain Charge			15		nC
Q_{oss}	Output Charge	V_{GS}=0V, V_{DS}=50V		134		nC
$t_{D(on)}$	Turn-On DelayTime	V_{GS}=10V, V_{DS}=50V, R_L=2.5Ω, R_{GEN}=3Ω		24		ns
t_r	Turn-On Rise Time			18		ns
$t_{D(off)}$	Turn-Off DelayTime			52		ns
t_f	Turn-Off Fall Time			22		ns
t_{rr}	Body Diode Reverse Recovery Time	I_F=20A, di/dt=500A/µs		45		ns
Q_{rr}	Body Diode Reverse Recovery Charge	I_F=20A, di/dt=500A/µs		287		nC

A. The value of $R_{\theta JA}$ is measured with the device mounted on 1in^2 FR-4 board with 2oz. Copper, in a still air environment with T_A =25° C. The Power dissipation P_{DSM} is based on R $_{\theta JA}$ t≤ 10s and the maximum allowed junction temperature of 150° C. The value in any given application depends on the user's specific board design.
B. The power dissipation P_D is based on $T_{J(MAX)}$=150° C, using junction-to-case thermal resistance, and is more useful in setting the upper dissipation limit for cases where additional heatsinking is used.
C. Single pulse width limited by junction temperature $T_{J(MAX)}$=150° C.
D. The $R_{\theta JA}$ is the sum of the thermal impedance from junction to case $R_{\theta JC}$ and case to ambient.
E. The static characteristics in Figures 1 to 6 are obtained using <300µs pulses, duty cycle 0.5% max.
F. These curves are based on the junction-to-case thermal impedance which is measured with the device mounted to a large heatsink, assuming a maximum junction temperature of $T_{J(MAX)}$=150° C. The SOA curve provides a single pulse rating.
G. The maximum current rating is package limited.
H. These tests are performed with the device mounted on 1 in^2 FR-4 board with 2oz. Copper, in a still air environment with T_A=25° C.

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TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS

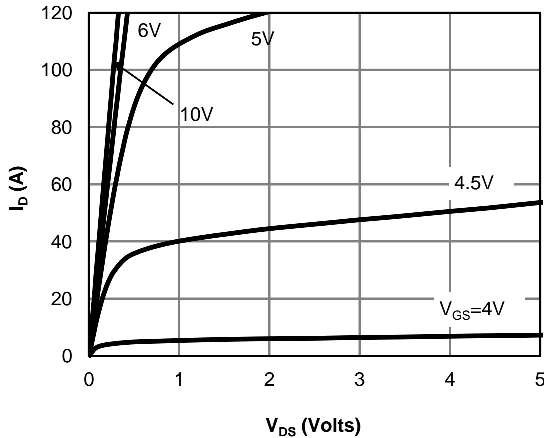

Figure 1: On-Region Characteristics (Note E)

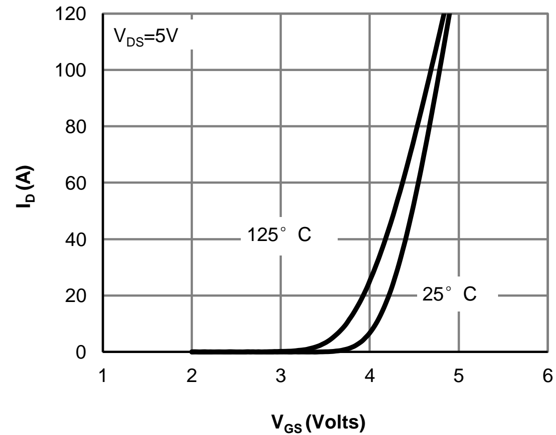

Figure 2: Transfer Characteristics (Note E)

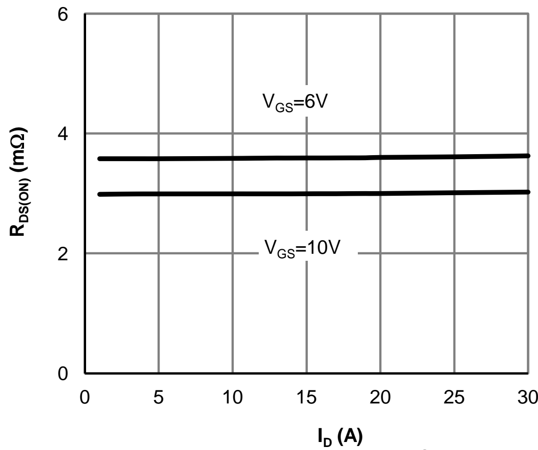

Figure 3: On-Resistance vs. Drain Current and Gate Voltage (Note E)

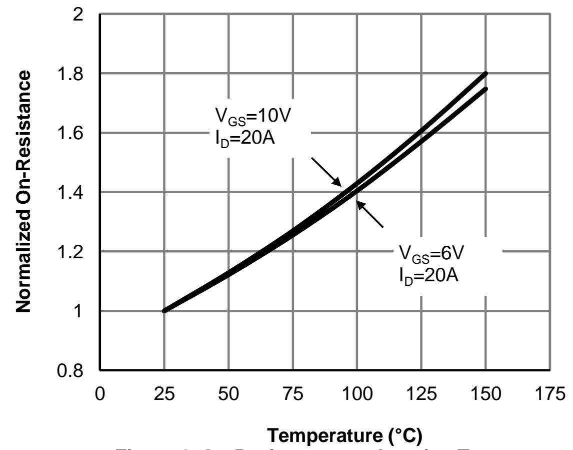

Figure 4: On-Resistance vs. Junction Temperature (Note E)

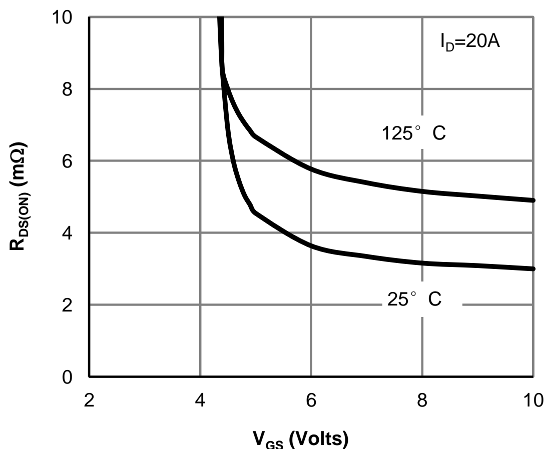

Figure 5: On-Resistance vs. Gate-Source Voltage (Note E)

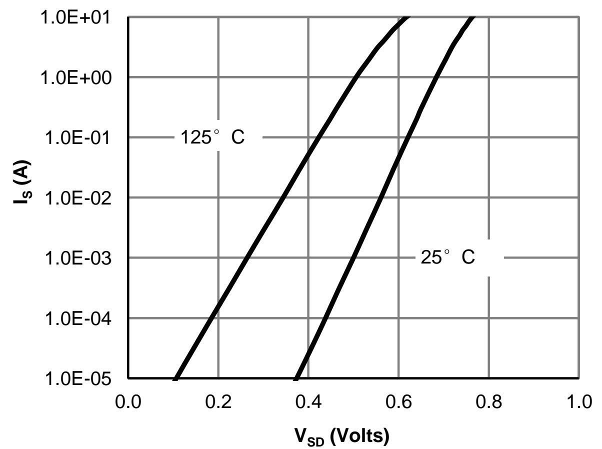

Figure 6: Body-Diode Characteristics (Note E)

TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS

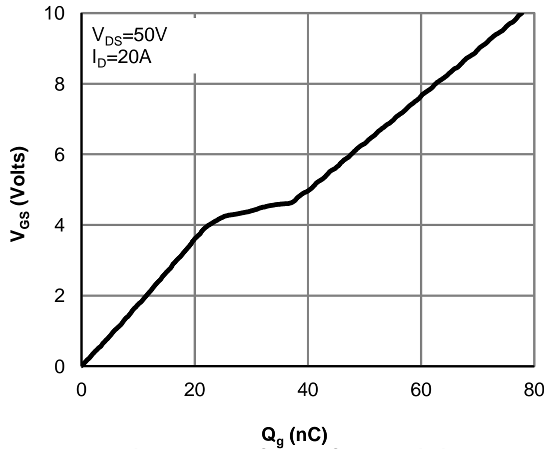

Figure 7: Gate-Charge Characteristics

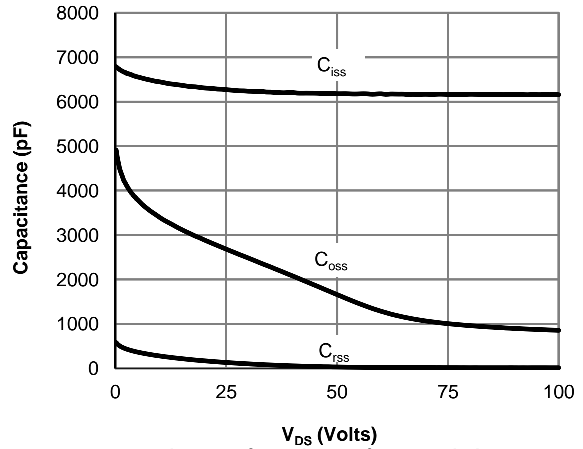

Figure 8: Capacitance Characteristics

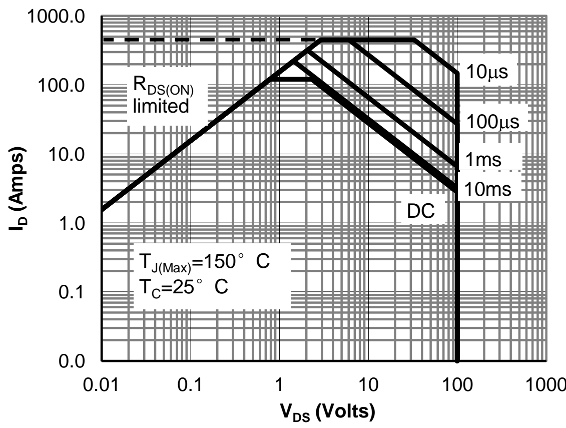

Figure 9: Maximum Forward Biased Safe Operating Area (Note F)

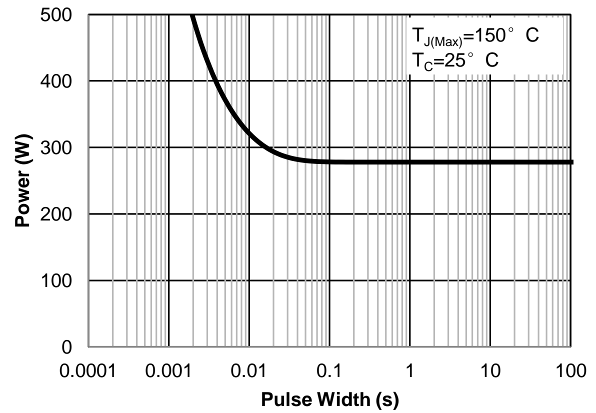

Figure 10: Single Pulse Power Rating Junction-to-Case (Note F)

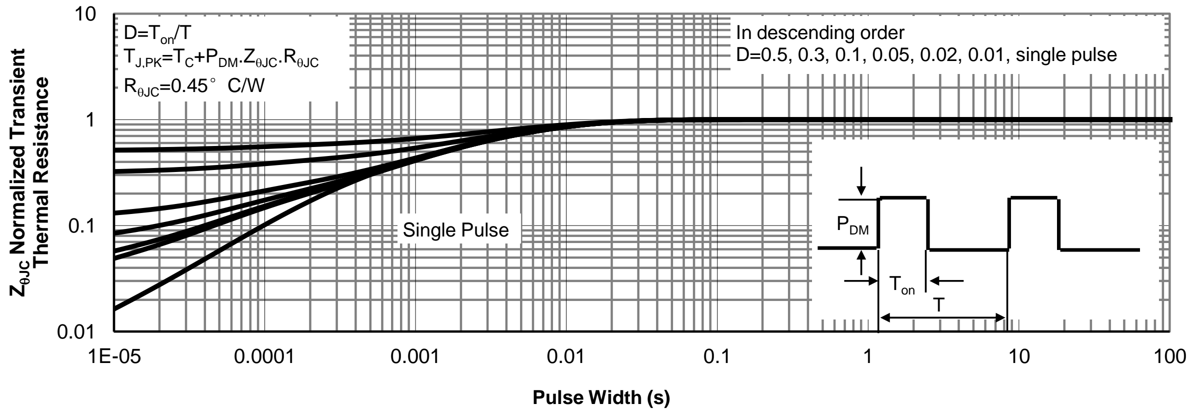

Figure 11: Normalized Maximum Transient Thermal Impedance (Note F)

TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS

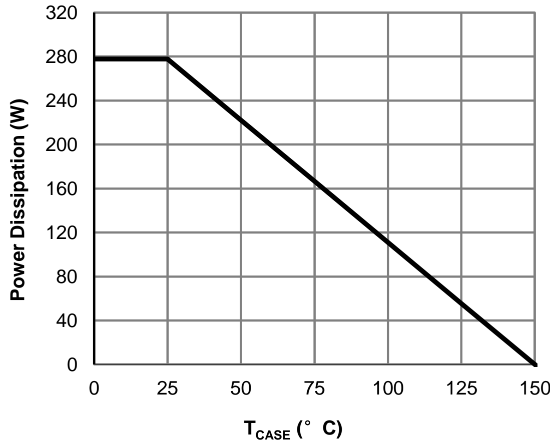

Figure 12: Power De-rating (Note F)

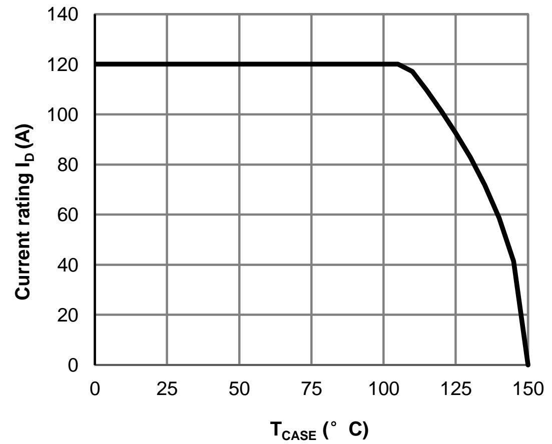

Figure 13: Current De-rating (Note F)

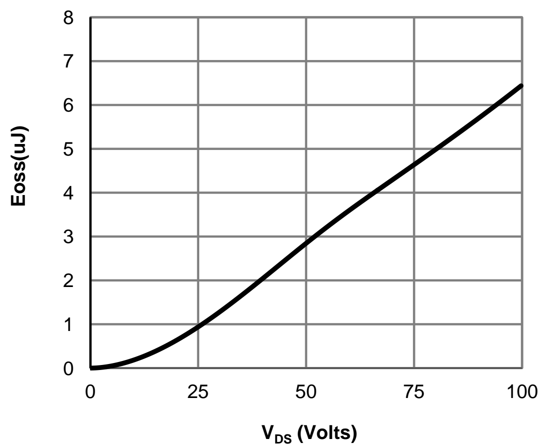

Figure 14: Coss stored Energy

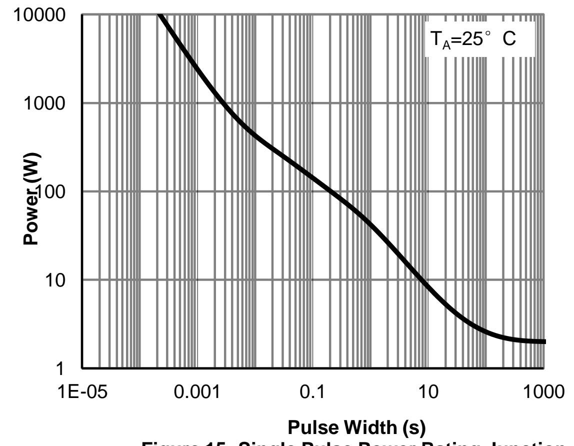

Figure 15: Single Pulse Power Rating Junction-to-Ambient (Note H)

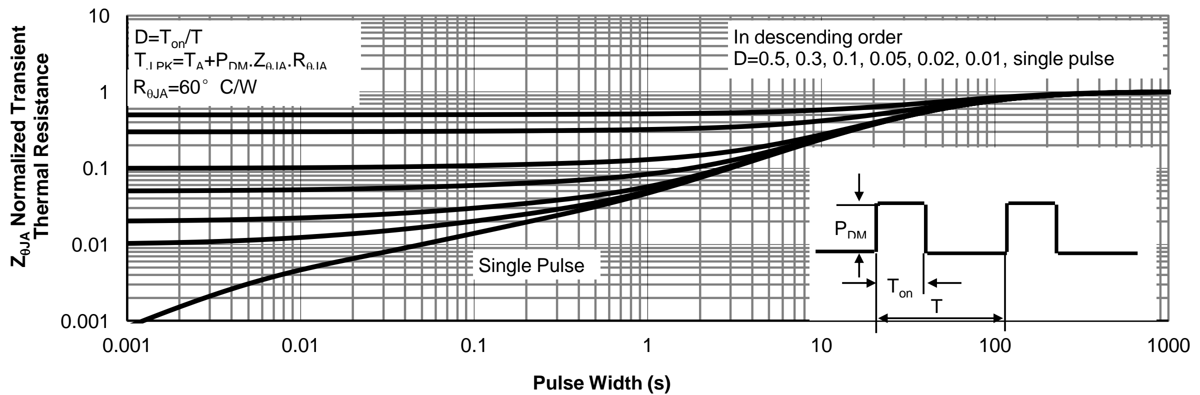

Figure 16: Normalized Maximum Transient Thermal Impedance (Note H)

Figure A: Gate Charge Test Circuit & Waveforms

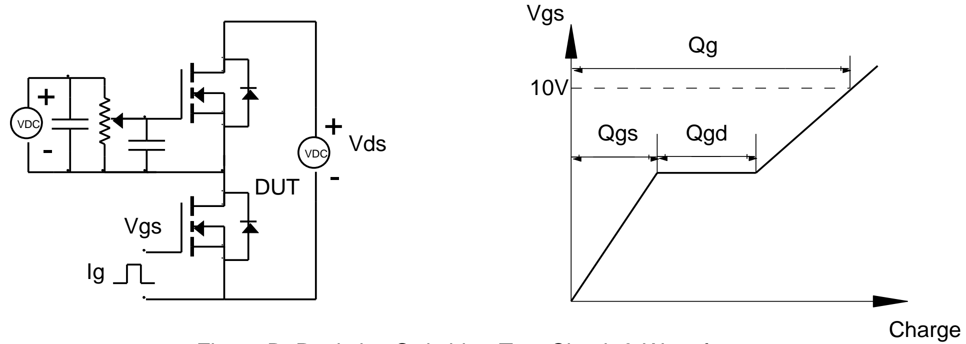

Figure B: Resistive Switching Test Circuit & Waveforms

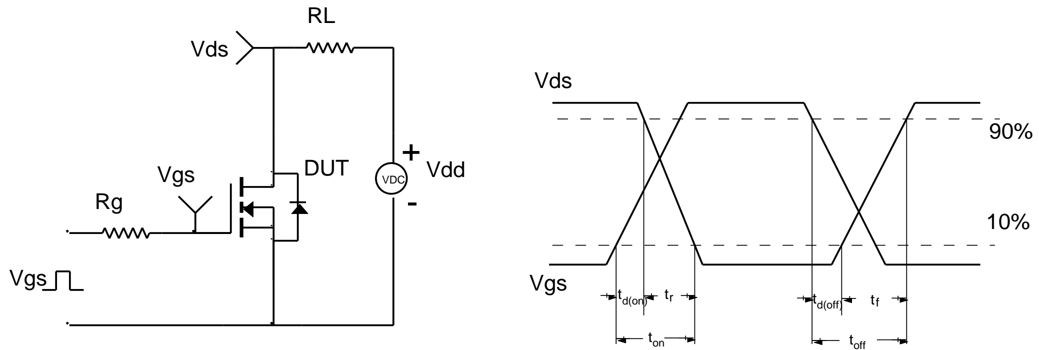

Figure C: Unclamped Inductive Switching (UIS) Test Circuit & Waveforms

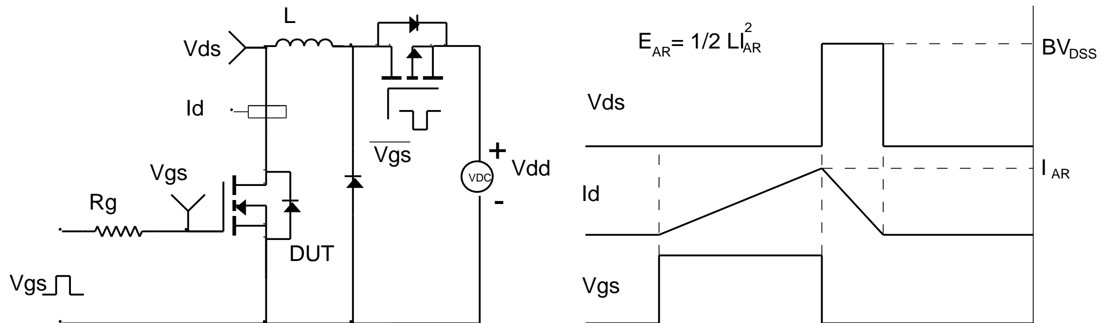

Figure D: Diode Recovery Test Circuit & Waveforms